

**PCN Number: RC140304**

**Notification Date\*:** February 19, 2014

<b>Title:</b> Migration to Marketing Revision Level B of the AT91SAM7X512																		
<b>Product Identification:</b>																		
		<table border="1" style="width:100%; border-collapse: collapse;"> <thead> <tr> <th style="width:50%;">Current Part Number</th> <th style="width:50%;">New Part Number</th> </tr> </thead> <tbody> <tr> <td>AT91SAM7X512-AU</td> <td>AT91SAM7X512B-AU</td> </tr> <tr> <td>AT91SAM7X512-AUR</td> <td>AT91SAM7X512B-AUR</td> </tr> <tr> <td>AT91SAM7X512-CU</td> <td>AT91SAM7X512B-CU</td> </tr> <tr> <td>AT91SAM7X512-CUR</td> <td>AT91SAM7X512B-CUR</td> </tr> </tbody> </table>		Current Part Number	New Part Number	AT91SAM7X512-AU	AT91SAM7X512B-AU	AT91SAM7X512-AUR	AT91SAM7X512B-AUR	AT91SAM7X512-CU	AT91SAM7X512B-CU	AT91SAM7X512-CUR	AT91SAM7X512B-CUR					
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AT91SAM7X512-CUR	AT91SAM7X512B-CUR																	
<b>Reason for Change:</b>	<input type="checkbox"/> Material / Composition <input checked="" type="checkbox"/> Processing / Manufacturing <input checked="" type="checkbox"/> Design / Firmware <input checked="" type="checkbox"/> Datasheet	<input type="checkbox"/> Manufacturing Location <input type="checkbox"/> Quality / Reliability <input type="checkbox"/> Logistics <input type="checkbox"/> Other:																
<b>Change Description:</b>																		
<p>A complete list of differences between the marketing revision level (MRL) A and B can be found in chapter 41.2 of the AT91SAM7X series datasheet with Atmel document reference 6120K.</p> <p>The ChipID has been incremented to:</p> <p style="padding-left: 40px;">AT91SAM7X512 Revision B chip ID is 0x275C 0A41</p> <p>The Flash memory access time has been reduced as per the below table:</p> <table border="1" style="width:100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width:25%;">Flash Wait State</th> <th style="width:25%;">Read Operations</th> <th style="width:50%;">Maximum Operating Frequency (MHz)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 cycle</td> <td style="text-align: center;">16</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">2 cycles</td> <td style="text-align: center;">32</td> </tr> <tr> <td style="text-align: center;">2</td> <td style="text-align: center;">3 cycles</td> <td style="text-align: center;">48</td> </tr> <tr> <td style="text-align: center;">3</td> <td style="text-align: center;">4 cycles</td> <td style="text-align: center;">55</td> </tr> </tbody> </table> <p>Samples are available in Atmel Sample Center:  <a href="https://samples.atmel.com/scripts/samplecenter.dll?atmel?cmd=menu">https://samples.atmel.com/scripts/samplecenter.dll?atmel?cmd=menu</a></p>				Flash Wait State	Read Operations	Maximum Operating Frequency (MHz)	0	1 cycle	16	1	2 cycles	32	2	3 cycles	48	3	4 cycles	55
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<b>Identification Method to Distinguish Change:</b>																		
Marketing Revision Level (MRL) has been incremented on the top side marking to C.																		
<b>Qualification Data:</b>	<input checked="" type="checkbox"/> Available	<input type="checkbox"/> Will be available (mm/dd/yr):	<input type="checkbox"/> Not Applicable															
<b>Samples:</b>	<input checked="" type="checkbox"/> Available	<input type="checkbox"/> Will be available (mm/dd/yr):	<input type="checkbox"/> Not Applicable															
<b>Quantifiable Impact on Quality &amp; Reliability:</b>																		
None																		

**Forecasted Availability Date:** February 20, 2014

**Last Time Buy Date:** May 20, 2014

**Last Ship Date:** February 20, 2015

*\*All orders placed after the notification date are non-cancellable and non-returnable (NCNR).*

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