ON Semiconductor

# Product Bulletin

Document # : PB21240X
Issue Date: 4 March 2016

| | |
|---|---|
| **Title of Change:** | Addressing of CAT24C04, CAT24C08 and CAT24C16 |
| **Effective date:** | 4 March 2016 |
| **Contact information:** | Contact your local ON Semiconductor Sales Office or <ovidiu.tol@onsemi.com> |
| **Type of notification:** | ON Semiconductor will consider this change accepted. |
| **Change category:** | ☐ Wafer Fab Change ☐ Assembly Change ☐ Test Change ☒ Other: ID page feature |

**Change Sub-Category(s):**

☐ Manufacturing Site Change/Addition
☐ Manufacturing Process Change
☐ Material Change
☒ Product specific change
☐ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

**Sites Affected:**

☐ All site(s) ☒ not applicable ☐ ON Semiconductor site(s) : ☐ External Foundry/Subcon site(s)

**Description and Purpose:**

For product shipped starting with Dec 2014 until Feb 2016 please refer to the description below:

**Bus contention**

Devices covered under this Product Bulletin will respond to the dedicated EEPROM Slave Address using pre-amble 1010 (Ah), and also to a Slave Address using pre-amble 1011 (Bh), where the latter is used for accessing an additional Identification Page. Therefore, if other devices sharing the $I^2C$ bus also respond to the latter Slave Address, then there will be bus contention, which in turn might cause a system error.

**Device addressing for devices with Page ID**

The Master initiates a data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address – as shown in the table below. For normal Read/Write operations to the memory array, the most significant 4 bits of the Slave Address (or pre-amble) are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices (listed below in upper case) and/or as internal address bits (listed below in lower case). The last bit of the slave address, R/W, specifies whether a Read (1) or Write (0) operation is to be performed. To access the additional Identification Page, the Slave Address pre-amble is fixed at 1011 (Bh) with the internal address bits (a10, a9, a8) as don't cares.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| CAT24C04 | Memory Array Access | 1 | 0 | 1 | 0 | A2 | A1 | a8 | R/W |
| | Identification Page Access | 1 | 0 | 1 | 1 | A2 | A1 | x | R/W |
| CAT24C08 | Memory Array Access | 1 | 0 | 1 | 0 | A2 | a9 | a8 | R/W |
| | Identification Page Access | 1 | 0 | 1 | 1 | A2 | x | x | R/W |
| CAT24C16 | Memory Array Access | 1 | 0 | 1 | 0 | a10 | a9 | a8 | R/W |
| | Identification Page Access | 1 | 0 | 1 | 1 | x | x | x | R/W |

For the customers having applications affected by this address feature, ON Semiconductor is ready to replace product with material not having this feature implemented.

**List of affected Parts:**

CAT24C04WI-GT3
CAT24C04WI-G
CAT24C04YI-GT3
CAT24C04YI-G
CAT24C04HU4I-GT3
CAT24C08WI-GT3
CAT24C08WI-G
CAT24C08YI-GT3
CAT24C08YE-GT3
CAT24C08YI-G
CAT24C08HU4I-GT3
CAT24C16WI-GT3
CAT24C16WE-GT3
CAT24C16WI-G
CAT24C16YI-GT3
CAT24C16YI-G
CAT24C16HU4I-GT3