W78E51C/W78E051C Data Sheet



8-BIT MICROCONTROLLER

Table of Contents-

1.	GENE	RAL DESCRIPTION		2
2.	FEAT	JRES		2
3.	PIN C	ONFIGURATIONS		3
4.	PIN D	SCRIPTION		4
5.			ON	
	5.1		eral	
	5.2	•	on	
	5.3			
	5.4	•		
	5.5			
	5.6	•		
6.	SECL			
	6.1			
	6.2			
	6.3			
7.	ELEC	• •	RISTICS	
	7.1		Ratings	
	7.2			
	7.3	A.C. Characteristics.		14
		7.3.1 Clock Input Wa	aveform	14
			n Cycle	
			cle	
		,	cle	
			ycleation	
8.	TIMIN		auori	
Ο.				
	8.1	-	e	
	8.2	•		
	8.3	•		
^	8.4 TVDI	•	DOLUTO	
9.			RCUITS	
	9.1	-	Program Memory and Crystal	
40	9.2	•	Data Memory and Oscillator	
10.				
	10.1	•		
	10.2	•		
4.4	10.3	•		
11.	KEVI:	ION HISTORY		23



1. GENERAL DESCRIPTION

The W78E051C is an 8-bit microcontroller which can accommodate a wider frequency range with low power consumption. The instruction set for the W78E051C is fully compatible with the standard 8051. The W78E051C contains an 4K bytes Flash EPROM; a 128 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit I/O port P4; two 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by seven sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E051C allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E051C microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

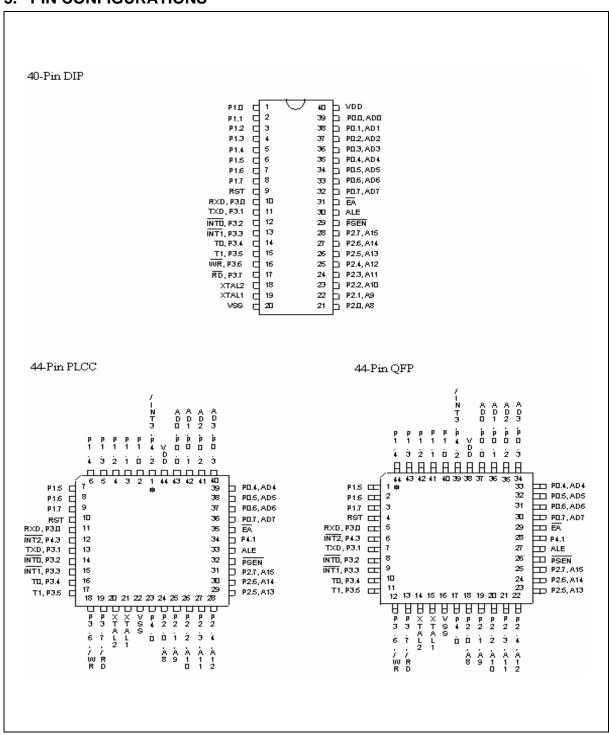
2. FEATURES

- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 4.5V to 5.5V
- 128 bytes of on-chip scratchpad RAM
- 4 KB On-chip Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- One extra 4-bit bit-addressable I/O port, additional INT2 / INT3 (available on 44-pin PLCC/QFP package)
- Two 16-bit timer/counters
- One full duplex serial port(UART)
- Watchdog Timer
- Seven sources, two-level interrupt capability
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:

Lead Free (RoHS) DIP 40: W78E051C40DL
Lead Free (RoHS) PLCC 44: W78E051C40PL
Lead Free (RoHS) PQFP 44: W78E051C40FL

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3. PIN CONFIGURATIONS



- 3 -

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4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
ĒĀ	EXTERNAL ACCESS ENABLE : This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and
EA	data will not be presented on the bus if \overline{EA} pin is high and the program counter is within on-chip ROM area.
PSEN	PROGRAM STORE ENABLE: PSEN enables the external ROM data onto the Port 0 address/ data bus during fetch and MOVC operations. When internal ROM access is performed, no PSEN strobe signal outputs from this pin.
ALE	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	RESET : A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.
Vss	GROUND: Ground potential
VDD	POWER SUPPLY: Supply voltage for operation.
P0.0-P0.7	PORT 0 : Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The pins of Port 0 are opendrain and should connect to pull up resistors if necessary while in programming.
	PORT 1 : Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below:
P1.0-P1.7	T2(P1.0): Timer/Counter 2 external count input
	T2EX(P1.1): Timer/Counter 2 Reload/Capture control
P2.0-P2.7	PORT 2 : Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
	PORT 3: Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port receiver input TXD(P3.1): Serial Port transmitter output
D0 0 D0 =	INTO (P3.2) : External Interrupt 0
P3.0-P3.7	INT1(P3.3): External Interrupt 1 T0(P3.4): Timer 0 External Input T1(P3.5): Timer 1 External Input
	WR (P3.6) : External Data Memory Write Strobe
	RD (P3.7) : External Data Memory Read Strobe
P4.0-P4.3	PORT 4: Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources (INT2/INT3).



5. FUNCTIONAL DESCRIPTION

The W78E051C architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 128 bytes of RAM, two timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

5.1 New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt INT2, INT3 has been added to either the PLCC or QFP 44 pin package. And description follows:

INT2/INT3

Two additional external interrupts, $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

1	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Seven-source interrupt information

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
External Interrupt 2	33H	5	XICON.2	XICON.0
External Interrupt 3	3BH	6 (lowest)	XICON.6	XICON.3

Publication Release Date: November 10, 2006 - 5 - Revision A4



Port 4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{\text{INT2}}$, $\overline{\text{INT3}}$).

Example:

P4 REG 0D8H

MOV P4, #0AH ; Output data "A" through P4.0–P4.3. MOV A, P4 ; Read P4 status to Accumulator.

ORL P4,#00000001B; Set bit P4.0 ANL P4,#11111101B; Clear bit P4.1

5.2 Reduce EMI Emission

Because of on-chip Flash EPROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is useless. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space. The AO bit in the AUXR register, when set, disables the ALE output. In order to reduce EMI emission from oscillation circuitry, W78E051C allows user to diminish the gain of on-chip oscillator amplifiers by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may effect to external crystal operating improperly at high frequency above 24 MHz. The value of R and C1, C2 may need adjustment while running at lower gain.

***AUXR - Auxiliary register (8EH)

AO: Turn off ALE output.

Power-off Flag

***PCON - Power control (87H)

-	_	_	POF	GF1	GF0	PD	IDL
				• • •	O . o		

POF: Power off flag. Bit is set by hardware when power on reset. It can be cleared by software to determine chip reset is a warm boot or cold boot.

GF1, GF0: These two bits are general-purpose flag bits for the user.

PD: Power down mode bit. Set it to enter power down mode.

IDL: Idle mode bit. Set it to enter idle mode.

The power-off flag is located at PCON.4. This bit is set when VDD has been applied to the part. It can be used to determine if a reset is a warm boot or a cold boot if it is subsequently reset by software.



5.3 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electromagnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit: 7 6 5 3 2 1 0 **ENW** PS₂ PS₁ **CLRW** WIDL PS₀ Mnemonic: WDTC Address: 8FH

ENW: Enable watch-dog if set.

CLRW: Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL: If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2~0 as follows:

PS2 PS1 PS0	PRESCALER SELECT
0 0 0	2
0 0 1	4
0 1 0	8
0 1 1	16
1 0 0	32
1 0 1	64
1 1 0	128
1 1 1	256

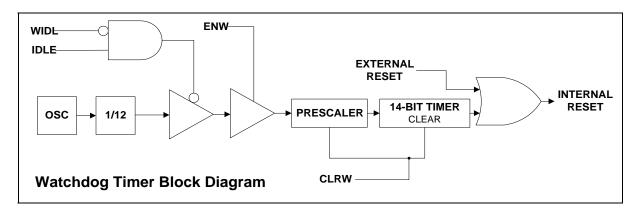
The time-out period is obtained using the following equation:

$$\frac{1}{OSC} \times 2^{14} \times PRESCALER \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.

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Typical Watch-dog time-out period when OSC = 20 MHz

PS2 PS1 PS0	WATCHDOG TIME-OUT PERIOD
0 0 0	19.66 mS
0 0 1	39.32 mS
0 1 0	78.64 mS
0 1 1	157.28 mS
1 0 0	314.57 mS
1 0 1	629.14 mS
1 1 0	1.25 S
1 1 1	2.50 S

5.4 Clock

The W78E051C is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78E051C relatively insensitive to duty cycle variations in the clock. The W78E051C incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.



5.5 Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

5.6 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E051C is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

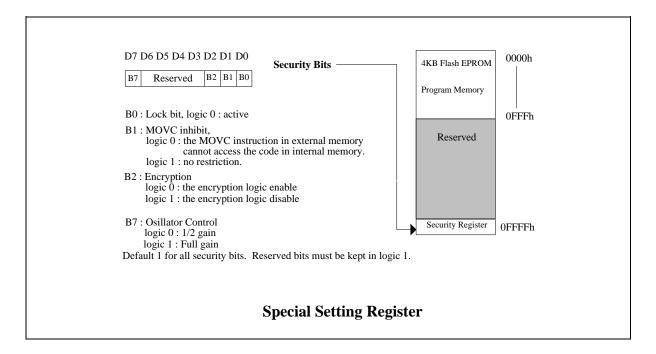
- 9 -

Publication Release Date: November 10, 2006 Revision A4



6. SECURITY BITS

During the programmer operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below. The W78E051C has a Special Setting Register, the Security Register, which can be accessed in normal mode. The register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



6.1 Lock Bit

This bit is used to protect the customer's program code in the W78E051C. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the on-chip ROM data and Special Setting Registers can not be accessed again.



6.2 MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

6.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

- 11 -

Publication Release Date: November 10, 2006 Revision A4



7. ELECREICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	VDD-VSS	-0.3	+7.0	V
Input Voltage	VIN	Vss -0.3	VDD +0.3	V
Operating Temperature	TA	0	70	°C
Storage Temperature	Тѕт	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 D.C. Characteristics

Vcc–Vss = 5V $\pm 10\%$, TA = 25° C, unless otherwise specified.

PARAMETER	SAMBOI	SYMBOL TEST CONDITIONS		SPECIFICATION	
TANAMETER	STINIBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Operating Voltage	VDD		4.5	5.5	V
Operating Current	IDD	No load VDD = 5.5V	-	20	mA
Idle Current	lidle	Idle mode VDD = 5.5V	-	6	mA
Power Down Current	IPWDN	Power-down mode VDD = 5.5V	-	50	μΑ
Input Current P1, P2, P3, P4	lin1	VDD = 5.5V VIN = 0V or VDD	-50	+10	μА
Logical 1-to-0 Transition Current P1, P2, P3 ^(*1) , P4	lτι	VDD = 5.5V $VIN = 2.0V$ (*1)	-550	-	μΑ
Input Current RST (*2)	IIN2	VDD = 5.5V VIN = VDD	-10	+300	μΑ
Input Leakage Current P0, EA	ILK	VDD = 5.5V 0V < VIN < VDD	-10	+10	μΑ
Output Low Voltage P1, P2, P3, P4	VOL1	VDD = 4.5V IOL1 = +2 mA	-	0.45	V
Output Low Voltage ALE, PSEN, P0 (*3)	VOL2	VDD = 4.5V IOL2 = +4 mA	-	0.45	V
Output High Voltage P1, P2, P3, P4	VOH1	VDD = 4.5V IOH1 = -100 μA	2.4	-	V

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DC Characteristics, continued

PARAMETER	SYMBOL	TEST CONDITIONS	SPECIFICATION		UNIT
TANAMETER	STWIBOL	1231 CONDITIONS	MIN.	MAX.	0111
Output High Voltage ALE, PSEN, P0 (*3)	VOH2	VDD = 4.5V IOH2 = -400 μA	2.4	-	٧
Input Low Voltage (Except RST)	VIL1	VDD = 4.5V	0	0.8	V
Input Low Voltage RST ^(*4)	VIL2	VDD = 4.5V	0	0.8	V
Input Low Voltage XTAL1 ^(*4)	VIL3	VDD = 4.5V	0	0.8	V
Input High Voltage (Except RST)	VIH1	VDD = 4.5V	2.4	VDD +0.2	V
Sink Current P1, P2, P3, P4	ISK1	VDD = 4.5V Vs = 0.45V	4	12	mA
Input High Voltage RST ^(*4)	VIH2	VDD = 4.5V	0.67 VDD	VDD +0.2	V
Input High Voltage XTAL1 ^(*4)	VIH3	VDD = 4.5V	0.67 VDD	VDD +0.2	V
Sink Current P0, ALE, PSEN (*3)	ISK2	VDD = 4.5V Vs = 0.45V	8	16	mA
Source Current P1, P2, P3, P4	ISR1	$VDD = 4.5V$ $V_S = 2.4V$	-100	-250	uA
Source Current P0, ALE, PSEN (*3)	ISR2	$VDD = 4.5V$ $V_s = 2.4V$	-8	-14	mA

Notes:

- 13 -

Publication Release Date: November 10, 2006 Revision A4

^{*1.} Pins P1, P2 and P3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN is approximately 2V.

^{*2.} RST pin has an internal pull-down resistor.

^{*3.} P0, ALE, PSEN are in the external access memory mode.

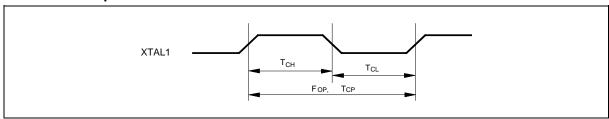
^{*4.} XTAL1 is a CMOS input and RST is a Schmitt trigger input.



7.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ± 20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

7.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	40	MHz	1
Clock Period	Тср	25	-	-	nS	2
Clock High	Тсн	10	-	-	nS	3
Clock Low	TCL	10	-	-	nS	3

Notes:

- 1. The clock may be stopped indefinitely in either state.
- 2. The Tcp specification is used as a reference in other specifications.
- 3. There are no duty cycle requirements on the XTAL1 input.

7.3.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 Tcp -Δ	ı	1	nS	4
Address Hold from ALE Low	Таан	1 Tcp -Δ	1	-	nS	1, 4
ALE Low to PSEN Low	TAPL	1 Tcp -∆	ı	-	nS	4
PSEN Low to Data Valid	TPDA	-	ı	2 TCP	nS	2
Data Hold after PSEN High	TPDH	0	•	1 Tcp	nS	3
Data Float after PSEN High	TPDZ	0	-	1 Tcp	nS	
ALE Pulse Width	TALW	2 Tcp -Δ	2 TCP	-	nS	4
PSEN Pulse Width	TPSW	3 TCP -∆	3 Тср	-	nS	4

Notes:

- 1. P0.0-P0.7, P2.0-P2.7 remain stable throughout entire memory cycle.
- 2. Memory access time is 3 Tcp.
- 3. Data have been latched internally prior to PSEN going high.
- 4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.



7.3.3 Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to RD Low	TDAR	3 Tcp -∆	-	3 TCP +∆	nS	1, 2
RD Low to Data Valid	TDDA	-	-	4 Tcp	nS	1
Data Hold from RD High	TDDH	0	-	2 Tcp	nS	
Data Float from RD High	TDDZ	0	-	2 Tcp	nS	
RD Pulse Width	TDRD	6 Tcp -∆	6 Тср	-	nS	2

Notes:

- 1. Data memory access time is 8 Tcp.
- 2. $^{"}\Delta"$ (due to buffer driving delay and wire loading) is 20 nS.

7.3.4 Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to WR Low	TDAW	3 Tcp -Δ	-	3 Tcp +∆	nS
Data Valid to WR Low	TDAD	1 Tcp -Δ	-	-	nS
Data Hold from WR High	Towd	1 Tcp -Δ	-	-	nS
WR Pulse Width	Towr	6 Tcp -Δ	6 Тср	-	nS

Note: "\Delta" (due to buffer driving delay and wire loading) is 20 nS.

7.3.5 Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 Tcp	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 Tcp	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

Publication Release Date: November 10, 2006 - 15 - Revision A4



7.3.6 Program Operation

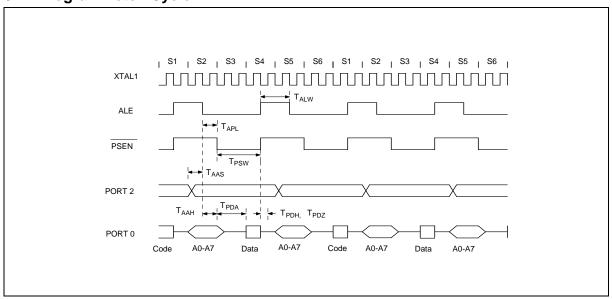
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VPP Setup Time	Tvps	2.0	-	-	μS
Data Setup Time	TDS	2.0	-	-	μS
Data Hold Time	TDH	2.0	-	-	μS
Address Setup Time	Tas	2.0	-	-	μS
Address Hold Time	Тан	0	-	-	μS
CE Program Pulse Width for Program Operation	TPWP	290	300	310	μS
OECTRL Setup Time	Tocs	2.0	-	-	μS
OECTRL Hold Time	Тосн	2.0	-	-	μS
OE Setup Time	Toes	2.0	-	-	μS
OE High to Output Float	TDFP	0	-	130	nS
Data Valid from OE	TOEV	-	-	150	nS

Note: Flash data can be accessed only in flash mode. The RST pin must pull in VIH status, the ALE pin must pull in VIL status, and the PSEN pin must pull in VIH status.

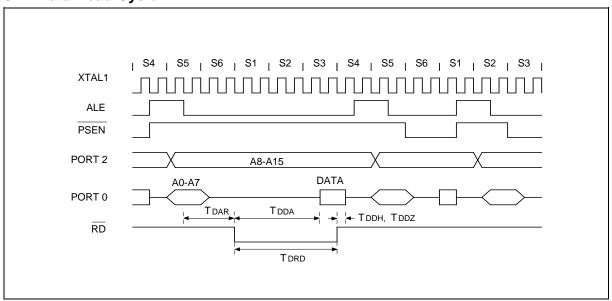


8. TIMING WAVEFORMS

8.1 Program Fetch Cycle



8.2 Data Read Cycle

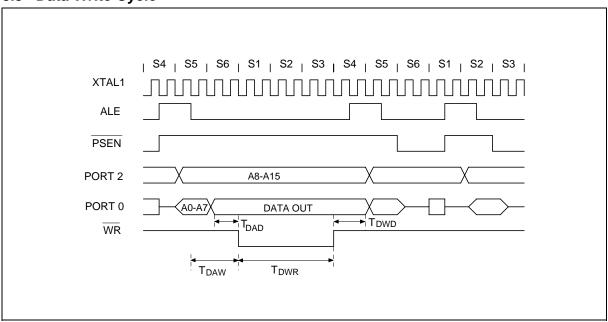


- 17 -

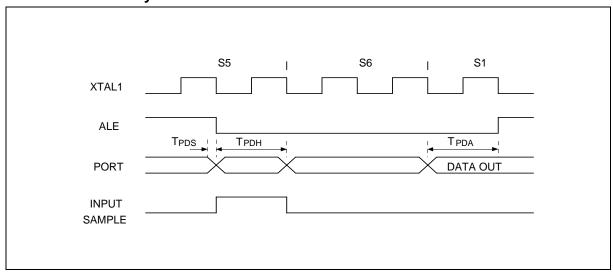


Timing Waveforms, continued

8.3 Data Write Cycle



8.4 Port Access Cycle





9. TYPICAL APPLICATION CIRCUITS

9.1 Expanded External Program Memory and Crystal

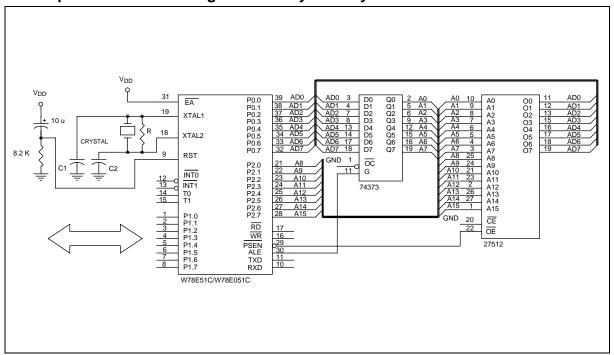


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
24 MHz	15P	15P	-
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications (full gain).

Note: C1, C2, R components refer to Figure A.



Typical Application Circuits, continued

9.2 Expanded External Data Memory and Oscillator

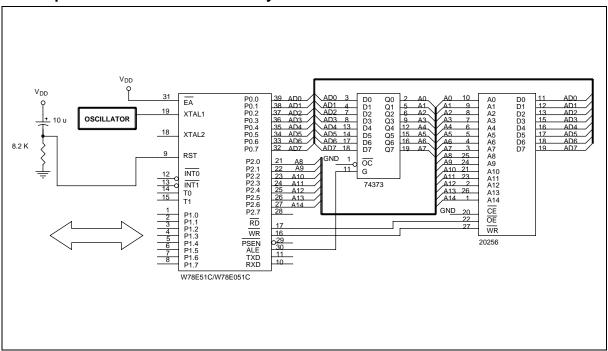
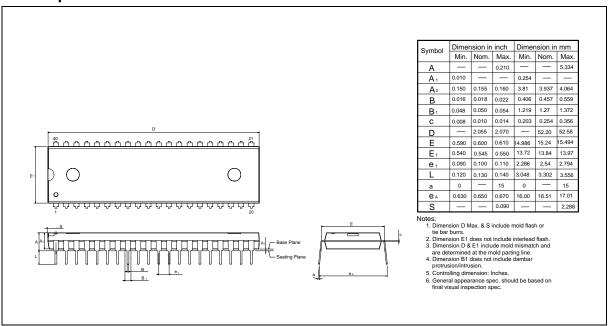


Figure B

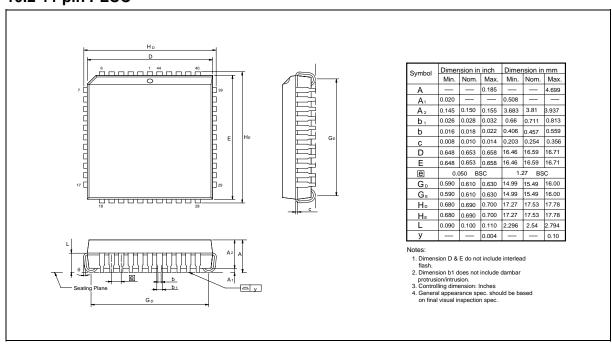


10. PACKAGE DIMENSIONS

10.1 40-pin DIP



10.2 44-pin PLCC

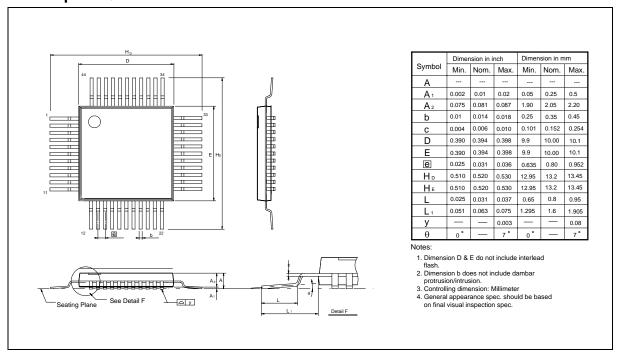


- 21 -



Package Dimensions, continued

10.3 44-pin PQFP





11. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 26, 2004	-	Formerly issued
A2	April 20, 2005	22	Add Important Notice
A3	May 16, 2005	2	Add Lead Free (RoHS) parts
A4 November 10, 2006		Remove block diagram	
	2006	2	Remove all Leaded parts

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