TLE7270-2

5-V Low Dropout Voltage Regulator

Automotive Power

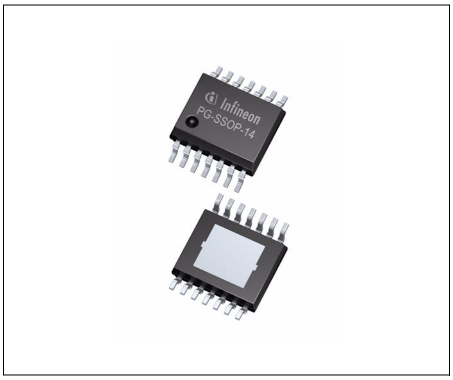
Never stop thinking

AEC Qualified RoHS

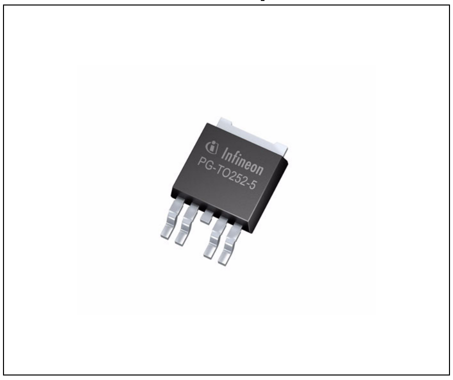
1 Overview

Features

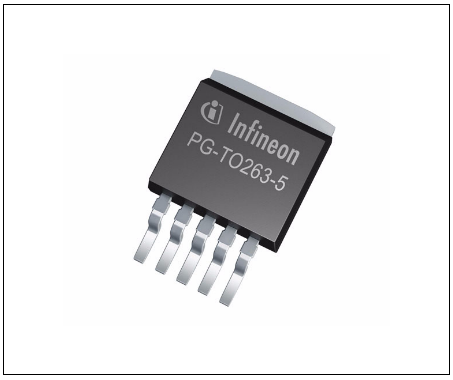
- Ultra Low Current Consumption 20 µA
- Output Voltage 5 V ±2%
- Output Current up to 300 mA
- Power-On and Undervoltage Reset
- Reset Low Down to V_Q = 1 V
- Very Low Dropout Voltage
- Output Current Limitation
- Overtemperature Shutdown
- Wide Temperature Range From -40 °C up to 150 °C
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-14 Exposed Pad



PG-TO252-5



PG-TO263-5

Description

The TLE7270-2 is a monolithic integrated low dropout voltage regulator for load currents up to 300 mA. An input voltage up to 42 V is regulated to $V_{Q,nom}$ = 5.0 V with a precision of ±2%. Due to its integrated reset circuitry featuring power on timing and output voltage monitoring the IC is well suited as µ-controller supply. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLE7270-2 can be also used in all other applications requiring a stabilized 5 V voltage.

Due to its ultra low quiescent current of typically 20 µA the TLE7270-2 is dedicated for use in applications permanently connected to V_{BAT}. An integrated output sink current circuitry keeps the voltage at the Output pin Q below 5.5 V even in case of occuring reverse currents. Thus connected devices are protected from overvoltage damage. For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XX and TLE 44XX is more suited than the TLE7270-2. A mV-range output noise on the TLE7270-2 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.

Type	Package	Marking
TLE7270-2E	PG-SSOP-14 Exposed Pad	7270-2E
TLE7270-2D	PG-TO252-5	7270-2D
TLE7270-2G	PG-TO263-5	7270-2G

2 Block Diagram

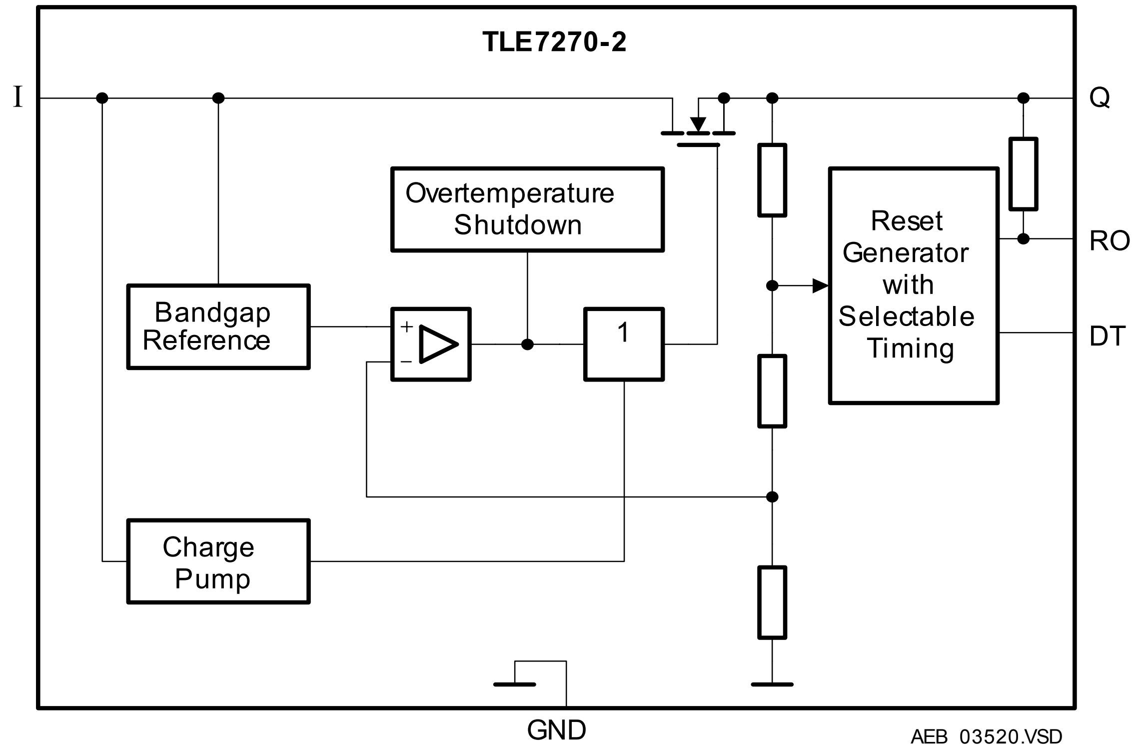


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment PG-SSOP-14 Exposed Pad

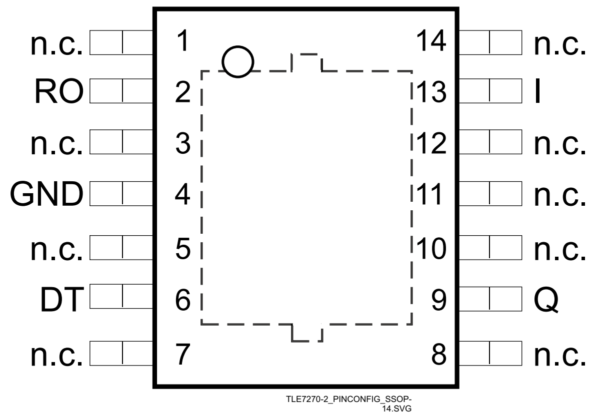


Figure 2 Pin Configuration (top view)

3.2 Pin Definitions and Functions PG-SSOP-14 Exposed Pad

Pin No.	Symbol	Function
1,3,5,7	n.c.	**non connected** can be open or connected to GND
2	RO	**Reset Output** open collector output with integrated pull-up resistor; optional external pull-up resistor of ≥ 10 kΩ to pin Q; leave open if reset function not needed
4	GND	**Ground**
6	DT	**Delay Timing** connect to GND or Q to choose the Power On Reset Delay Time
8,10,11,12,14	n.c.	**non connected** can be open or connected to GND
9	Q	**Output** block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in **"Functional Range" on Page 6**
13	I	**Input** block to ground directly at the IC with a ceramic capacitor
Pad	–	**Exposed Pad** connect to GND and heatsink area

3.3 Pin Assignment PG-TO252-5, PG-TO263-5

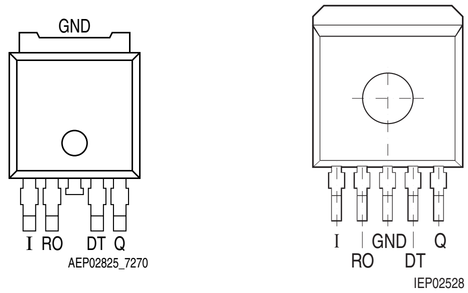


Figure 3 Pin Configuration (top view)

3.4 Pin Definitions and Functions PG-TO252-5, PG-TO263-5

Pin No.	Symbol	Function
1	I	**Input** block to ground directly at the IC with a ceramic capacitor
2	RO	**Reset Output** open collector output with integrated pull-up resistor; optional external pull-up resistor of ≥ 10 kΩ to pin Q; leave open if reset function not needed
3	GND	**Ground** internally connected to heat slug
4	DT	**Delay Timing** connect to GND or Q to choose the Power On Reset Delay Time
5	Q	**Output** block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in **“Functional Range” on Page 6**
Heat Slug	–	**Heat Slug** internally connected to GND; connect to GND and heatsink area

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]
T_j = -40 °C to 150 °C; all voltages with respect to ground, (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Condition
			Min.	Max.		
Input I						
4.1.1	Voltage	V_I	-0.3	45	V	–
Output Q, Reset Output RO, Delay Time DT						
4.1.2	Voltage	V_Q, V_{RO}, V_{DT}	-0.3	6	V	–
4.1.3	Voltage	V_Q, V_{RO}, V_{DT}	-0.3	6.2	V	t < 10 s[2)]
Temperature						
4.1.4	Junction temperature	T_j	-40	150	°C	–
4.1.5	Storage temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
4.1.6	Human Body Model (HBM)[3)]	Voltage	-	3	kV	–
4.1.7	Charged Device Model (CDM)[4)]	Voltage	-	1.5	kV	–

1) not subject to production test, specified by design
2) exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability
3) ESD susceptibility Human Body Model "HBM" according to AEC-Q100-002 - JESD22-A114
4) ESD susceptibility Charged Device Model "CDM" according to ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
4.2.1	Input voltage	V_I	5.5	42	V	–
4.2.2	Output Capacitor's Requirements	C_Q	470	–	nF	1)
4.2.3		$ESR(C_Q)$	–	10	Ω	2)
4.2.4	Junction temperature	T_j	-40	150	°C	–

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%
2) relevant ESR value at f = 10 kHz

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
TLE7270-2E (PG-SSOP-14 Exposed Pad)							
4.3.1	Junction to Case[1]	R_{thJC}	–	14	–	K/W	measured to exposed pad
4.3.2	Junction to Ambient[1]	R_{thJA}	–	47	–	K/W	[2]
4.3.3		R_{thJA}	–	141	–	K/W	footprint only[3]
4.3.4		R_{thJA}	–	66	–	K/W	300 mm² heatsink area[3]
4.3.5		R_{thJA}	–	56	–	K/W	600 mm² heatsink area[3]
TLE7270-2D (PG-TO252-5)							
4.3.1	Junction to Case[1]	R_{thJC}	–	6	–	K/W	measured to tab
4.3.2	Junction to Ambient[1]	R_{thJA}	–	32	–	K/W	[2]
4.3.3		R_{thJA}	–	115	–	K/W	footprint only[3]
4.3.4		R_{thJA}	–	62	–	K/W	300 mm² heatsink area[3]
4.3.5		R_{thJA}	–	47	–	K/W	600 mm² heatsink area[3]
TLE7270-2G (PG-TO263-5)							
4.3.1	Junction to Case[1]	R_{thJC}	–	6	–	K/W	measured to exposed pad
4.3.2	Junction to Ambient[1]	R_{thJA}	–	27	–	K/W	[2]
4.3.3		R_{thJA}	–	75	–	K/W	footprint only[3]
4.3.4		R_{thJA}	–	47	–	K/W	300 mm² heatsink area[3]
4.3.5		R_{thJA}	–	38	–	K/W	600 mm² heatsink area[3]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a $76.2 \times 114.3 \times 1.5$ mm³ board with 1 copper layer (1 x 70µm Cu).

5 Electrical Characteristics

5.1 Electrical Characteristics Voltage Regulator

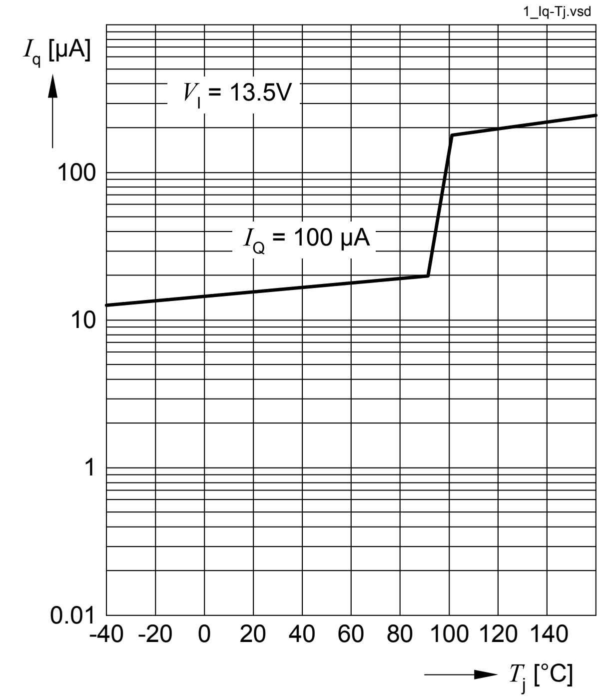
Electrical Characteristics
V_I=13.5 V; T_j = -40 °C to 150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Measuring Condition
			Min.	Typ.	Max.		
Output Q							
5.1.1	Output Voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q<300 mA 6 V < V_I < 16 V
5.1.2	Output Voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q<100 mA 6 V < V_I < 40 V
5.1.3	Dropout Voltage	V_{dr}	–	250	500	mV	I_Q = 200 mA $V_{dr} = V_I - V_Q$ 1)
5.1.4	Load Regulation	$\Delta V_{Q, lo}$	– 40	15	40	mV	I_Q = 5 mA to 250 mA
5.1.5	Line Regulation	$\Delta V_{Q, li}$	– 20	5	20	mV	V_I = 10 V to 32 V I_Q = 5 mA
5.1.6	Output Current Limitation	I_Q	301	–	–	mA	1)
5.1.7	Output Current Limitation	I_Q	–	–	800	mA	V_Q = 0V
5.1.8	Power Supply Ripple Rejection 2)	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
5.1.9	Temperature Output Voltage Drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–
Current Consumption							
5.1.10	Quiescent Current $I_q = I_I - I_Q$	I_q	–	20	30	µA	I_Q = 0.1 mA T_j = 25 °C
5.1.11	Quiescent Current $I_q = I_I - I_Q$	I_q	–	–	40	µA	I_Q = 0.1 mA $T_j \leq$ 80 °C

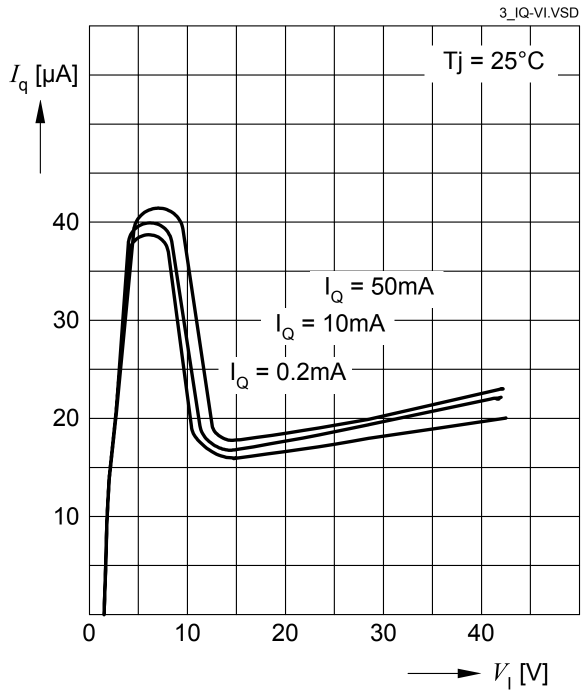
1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.
2) not subject to production test, specified by design

5.2 Typical Performance Characteristics Voltage Regulator

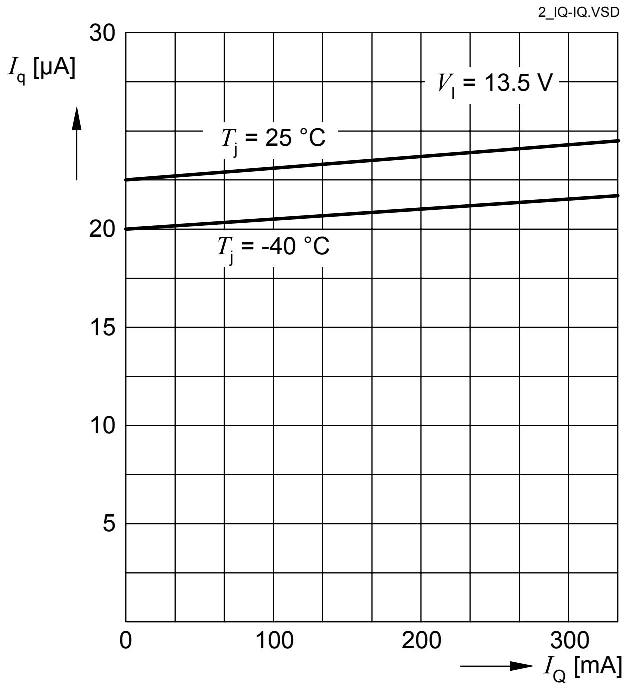
Current Consumption I_q versus Junction Temperature T_J



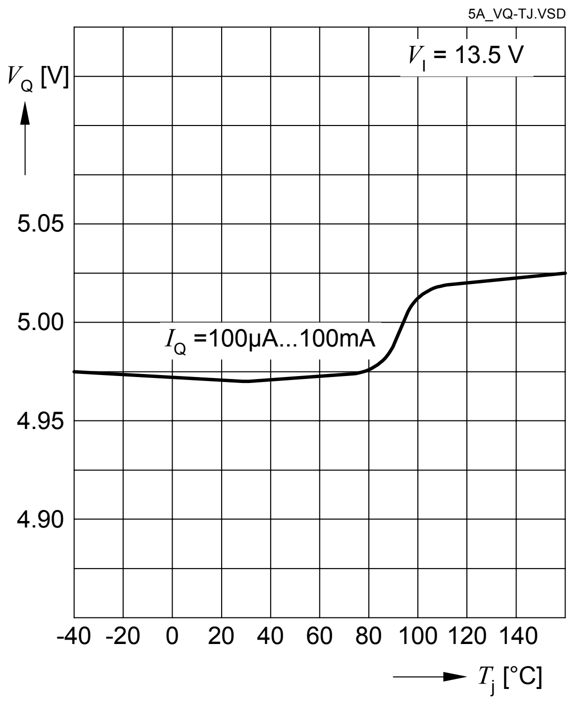
Current Consumption I_q versus Input Voltage V_{IQ}



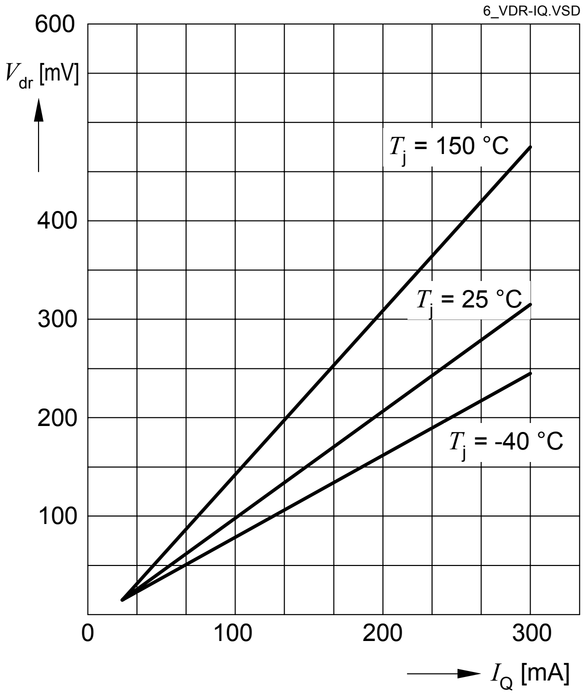
Current Consumption I_q versus Output Current I_Q



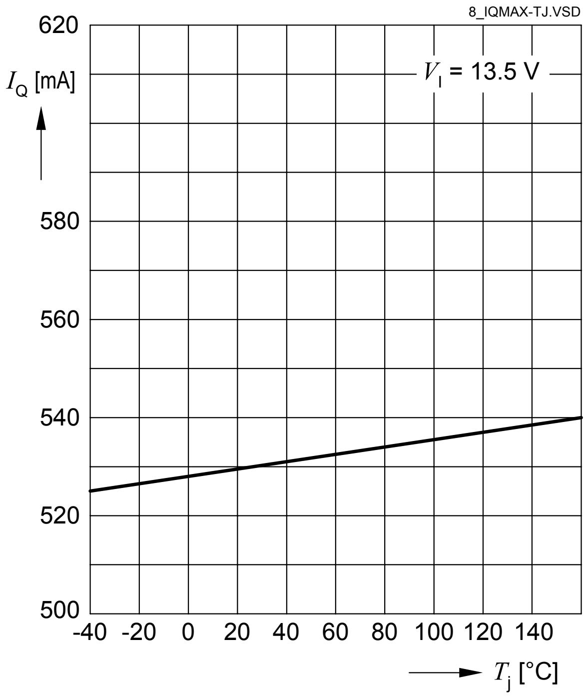
Output Voltage V_Q versus Junction Temperature T_J



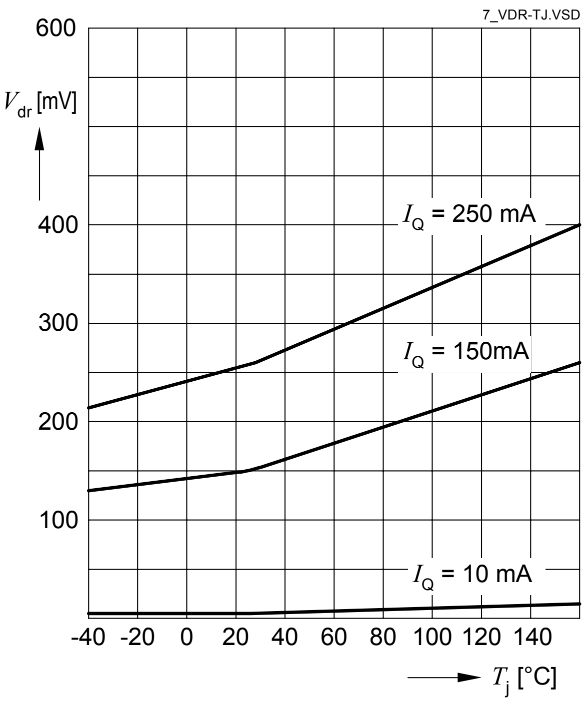
Dropout Voltage V_{dr} versus Output Current I_Q



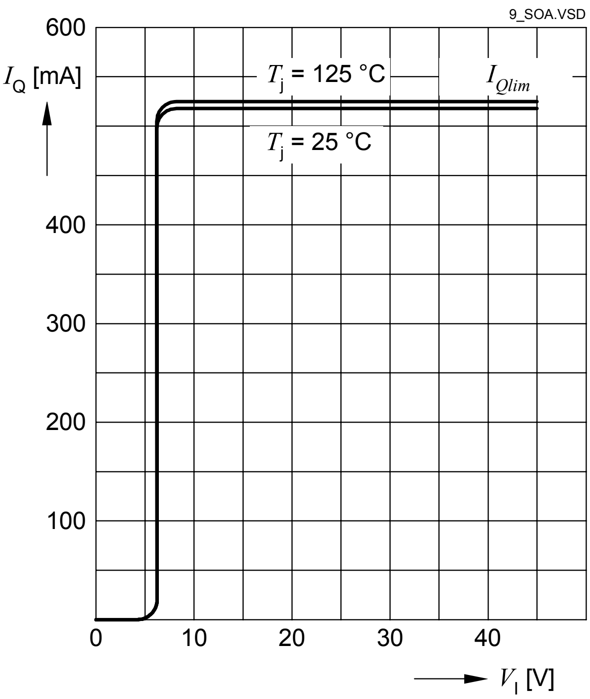
Maximum Output Current I_Q versus Junction Temperature T_j



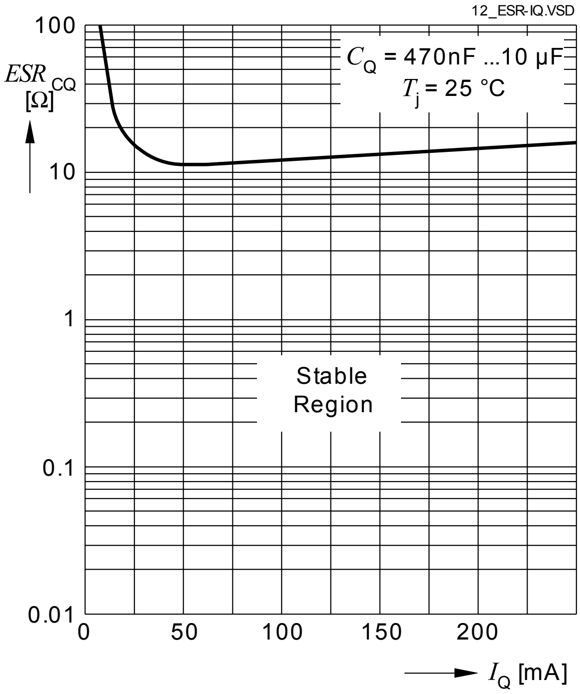
Dropout Voltage V_{dr} versus Junction Temperature



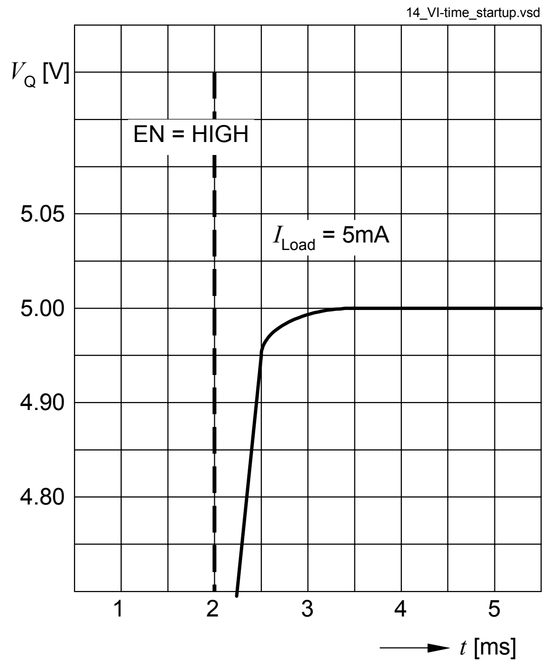
Maximum Output Current I_Q versus Input Voltage V_I



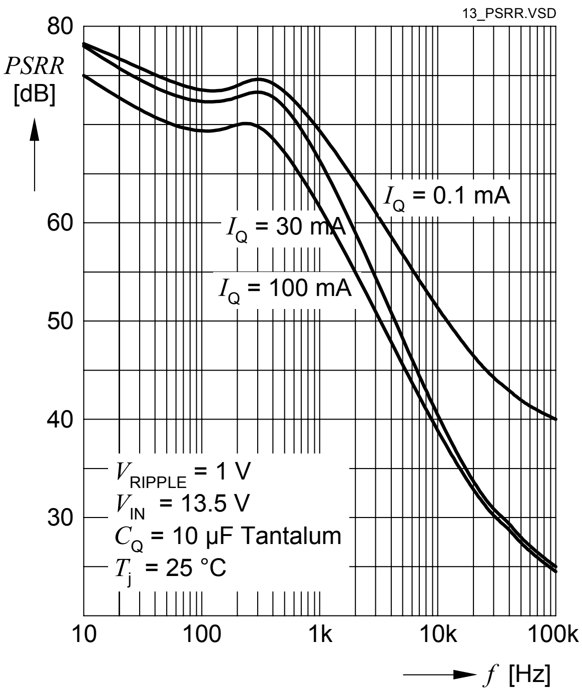
Region of Stability



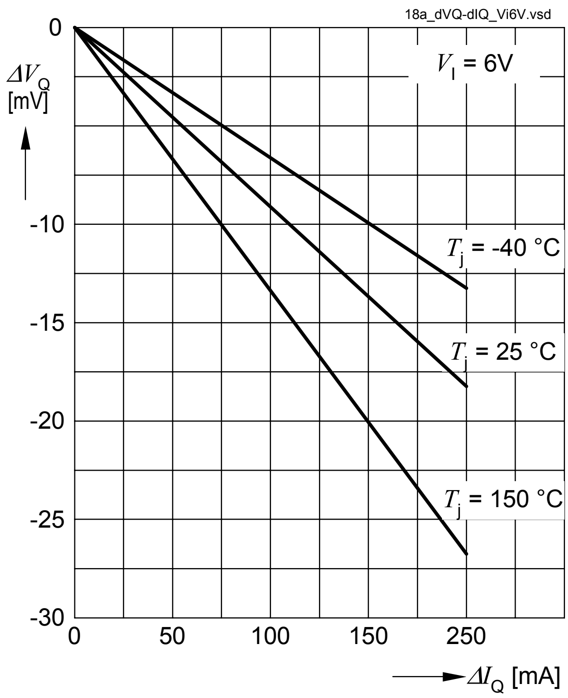
Output Voltage V_Q Start-up behavior



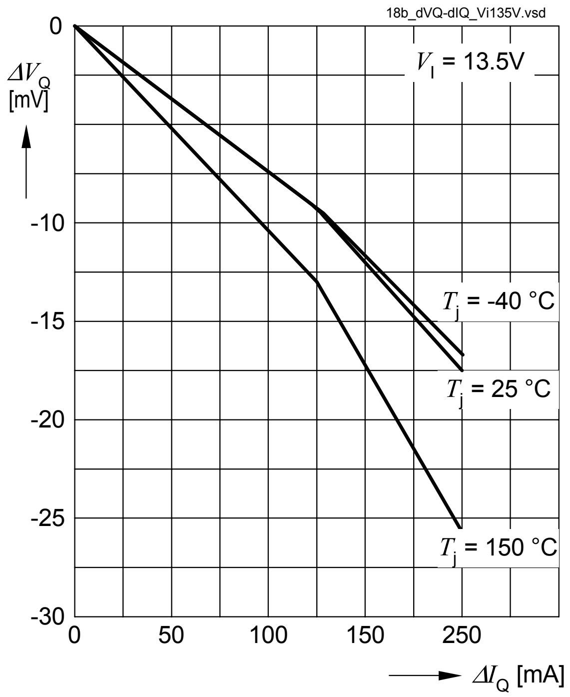
Power Supply Ripple Rejection PSRR versus Frequency f



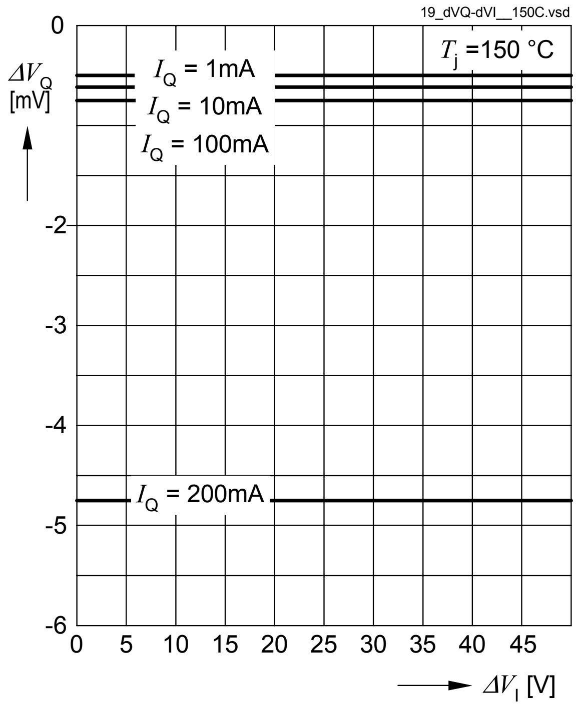
Load Regulation ΔV_Q versus Output Current Change ΔI_Q



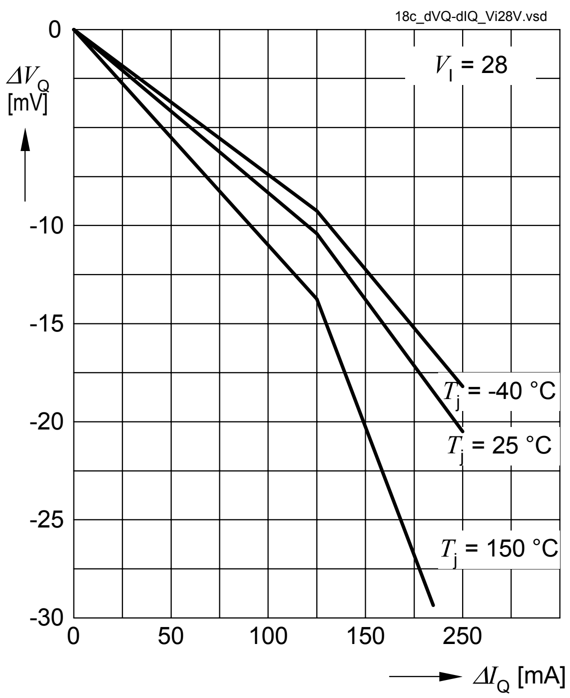
Load Regulation ΔV_Q versus Output Current Change dI_Q



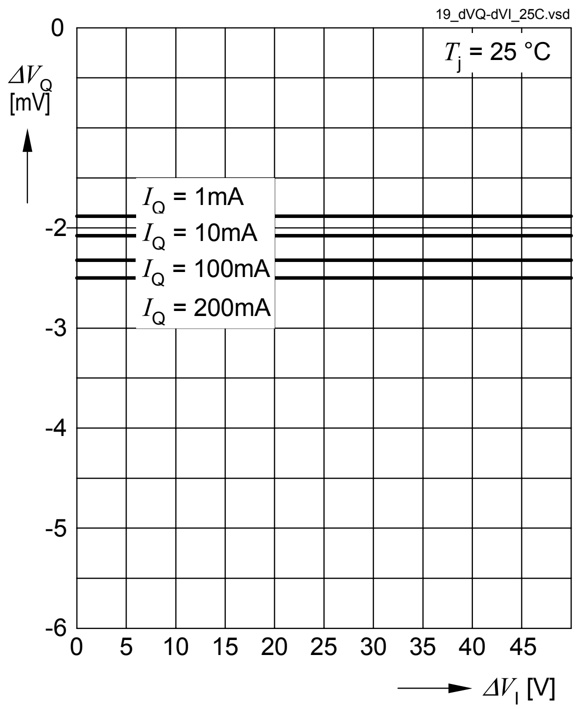
Line Regulation ΔV_Q versus Input Voltage Changed V_I



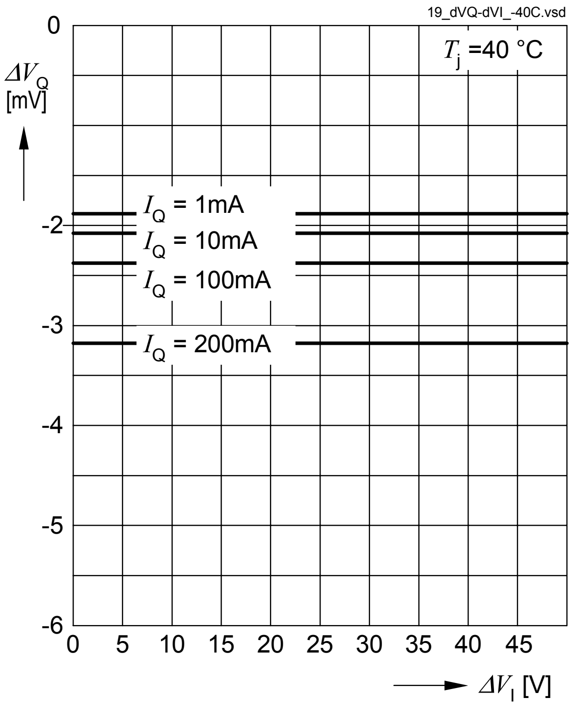
Load Regulation ΔV_Q versus Output Current Change ΔI_Q



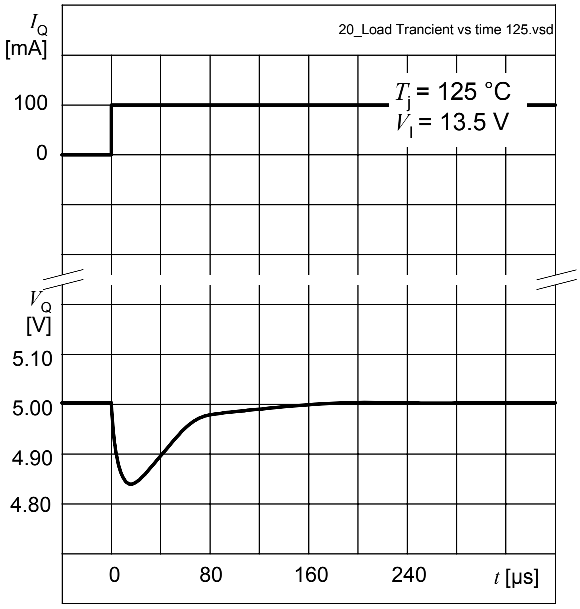
Line Regulation ΔV_Q versus Input Voltage Changed V_I



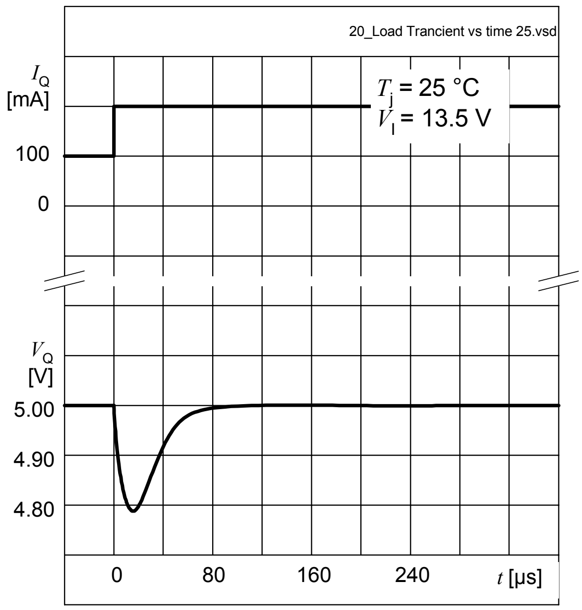
Line Regulation ΔV_Q versus Input Voltage Change V_I



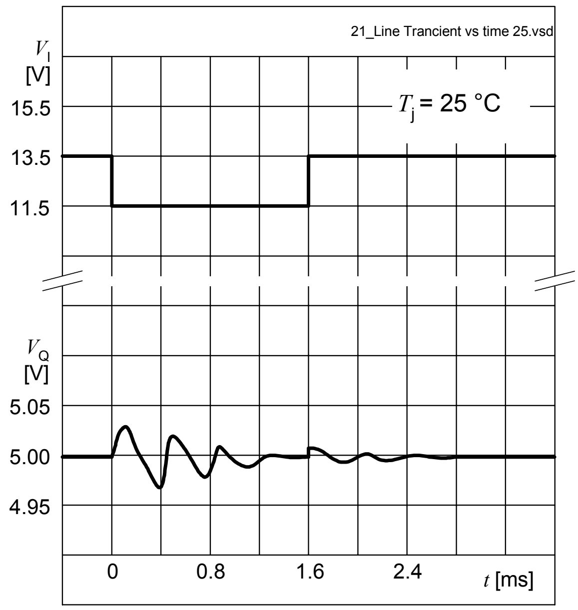
Load Transient Response Peak Voltage ΔV_Q



Load Transient Response Peak Voltage ΔV_Q

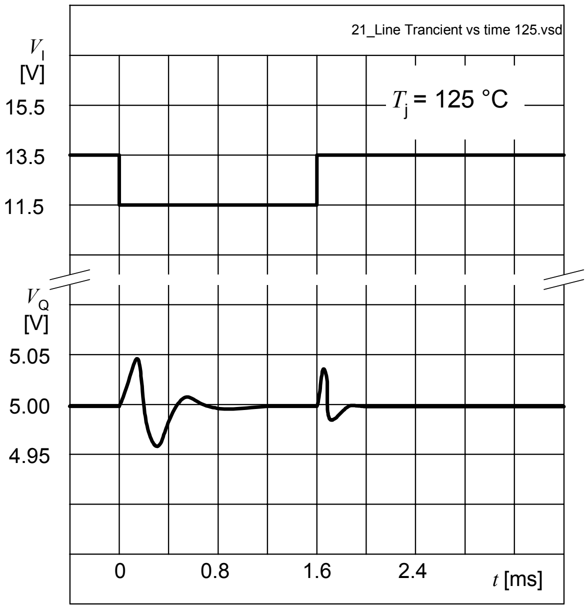


Line Transient Response Peak Voltage ΔV_Q



Line Transient Response Peak Voltage ΔV_Q

I



5.3 Electrical Characteristics Reset Function

The Reset function informs e.g. the microcontroller in case the output voltage has fallen below the lower threshold **VRT** of typ. 4.65 V. The headroom **VRH** between the output voltage and the reset threshold is typically 350 mV. Connecting the regulator to a battery voltage at first the reset signal remains LOW. When the output voltage has reached the reset threshold **VRT** the reset output RO remains still LOW for the reset delay time **tRD**. Afterwards the reset output turns HIGH.

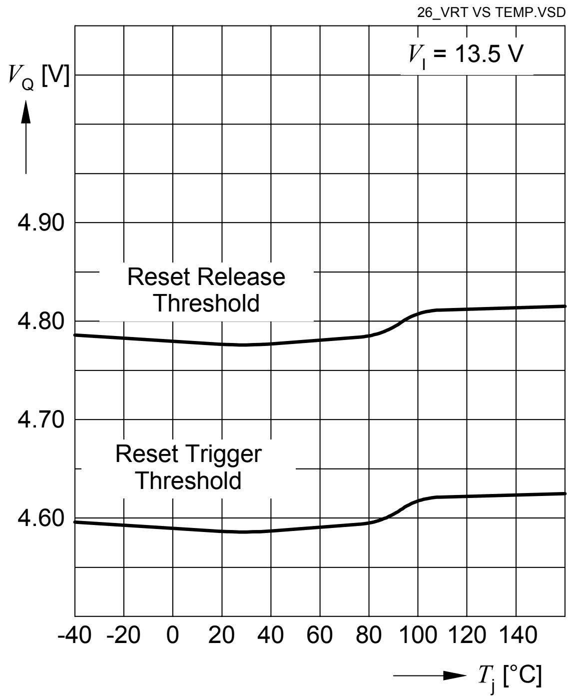
Electrical Characteristics Reset

V_I=13.5 V; – 40 °C < T_j < 150 °C; all voltages with respect to ground (unless otherwise specified)

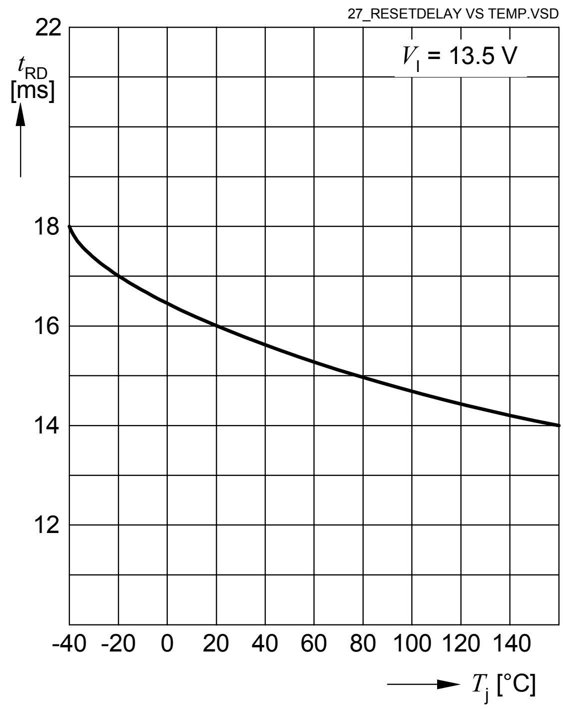
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Output Undervoltage Reset Switching Threshold	V_{RT}	4.50	4.65	4.80	V	V_Q decreasing V_I = 6V
5.3.2	Output Undervoltage Reset Headroom	V_{RH}	–	350	–	mV	–
5.3.3	Reset Output Low Level Voltage	V_{ROL}	–	0.2	0.4	V	R_{RO} = 10 kΩ; V_Q > 1 V
5.3.4	Integrated Reset Pull Up Resistor	R_{RO}	15	30	45	kΩ	–
5.3.5	Optional External Reset Pull Up Resistor	$R_{RO,ext}$	10	–	–	kΩ	–
5.3.6	Power On Reset Delay Time	t_{RD}	10	16	22	ms	pin DT connected to GND
5.3.7	Power On Reset Delay Time	t_{RD}	80	128	176	ms	pin DT connected to Q
5.3.8	Reset Reaction Time	t_{RR}	–	–	12	µs	–

5.4 Typical Performance Characteristics Reset Function

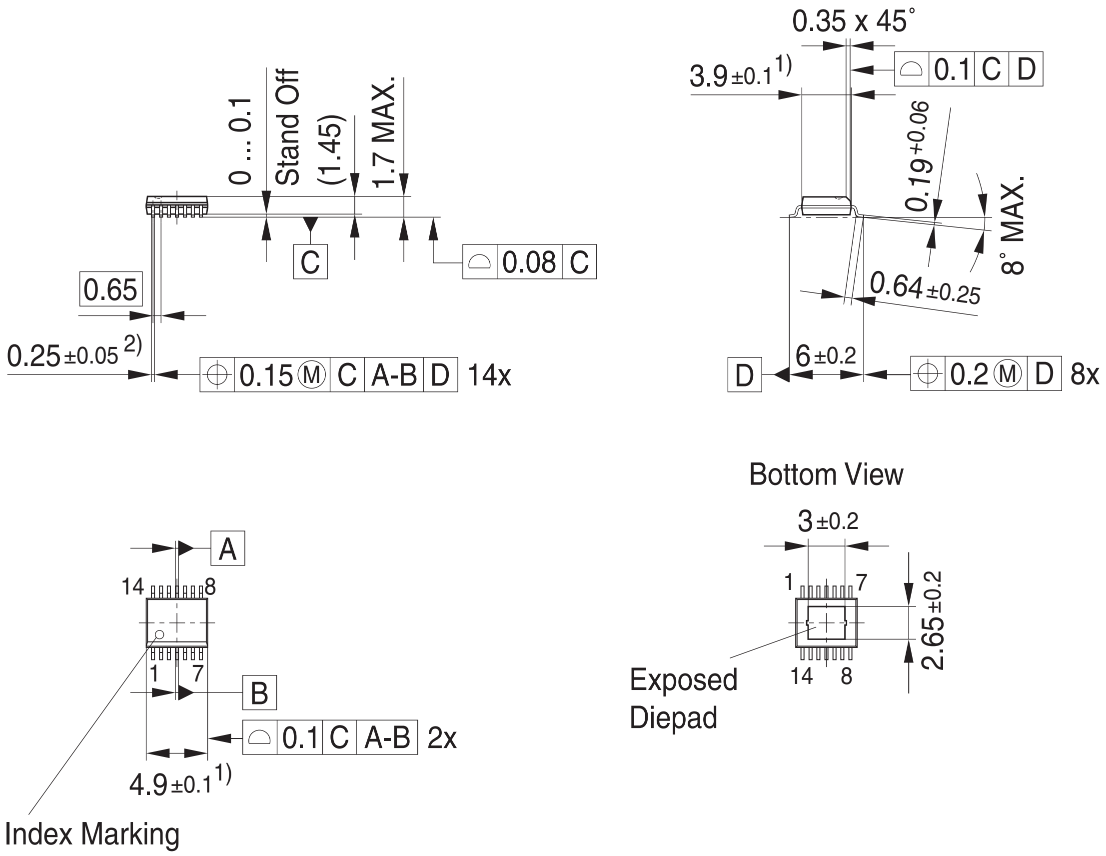
Reset Threshold V_{RT} versus Junction Temperature T_J



Reset Delay t_{RD} versus Junction Temperature T_J at fast timing (DT connected to GND)



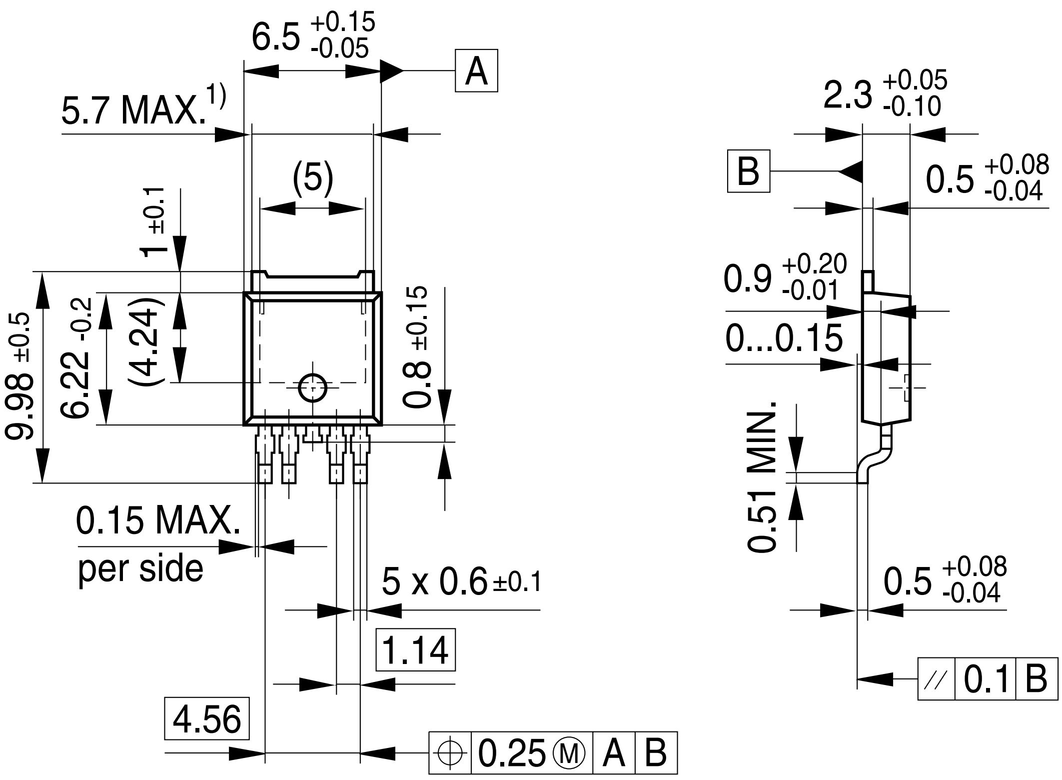
6 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

PG-SSOP-14-1,-2,-3-PO V02

Figure 4 PG-SSOP-14 Exposed Pad



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

Figure 5 PG-TO252-5

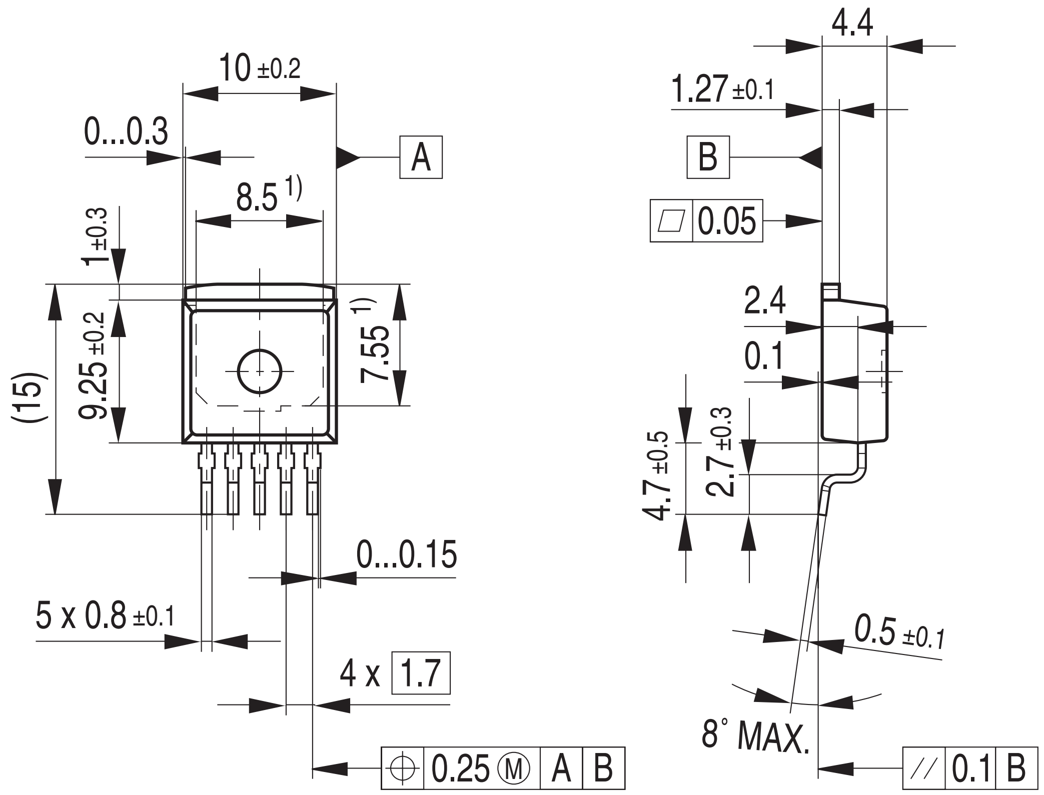


Figure 6 PG-TO263-5

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

7 Revision History

Revision	Date	Changes
1.01	2009-07-23	updated version data sheet:
		in **"Electrical Characteristics Voltage Regulator" on Page 8**, former Item 5.1.12 "Current Consumption, Regulator Disabled" removed, in Condition of **Item 5.1.10** and **Item 5.1.11** "V_{EN} = 5 V" removed: Non relevant information as TLE7270-2 does not implement Enable Feature
1.0	2009-06-01	initial version data sheet

Edition 2009-07-23

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